User's Guide
SNVA323B–March 2008–Revised May 2013

AN-1786 LM2854 500 kHz Buck Regulator Evaluation Board

1 Introduction

The LM2854 PowerWise® SIMPLE SWITCHER® buck regulator evaluation board is a 500 kHz step-down voltage regulator capable of driving up 0A to 4A load current with excellent power conversion efficiency. A typical schematic of an LM2854 application is given in Figure 1. The LM2854 pin-out and pin description are given in Figure 2 and Table 1, respectively.

The LM2854 evaluation board is designed to accept an input voltage rail between 2.95V and 5.5V and deliver a fixed and highly accurate output voltage of 1.2V. The output voltage level can be changed by modification of the one feedback resistor value. Externally established soft-start with a small value capacitance facilitates a controlled, well-defined and monotonic start-up output voltage characteristic. In addition, the LM2854 is capable of starting monotonically and glitch free into a pre-biased load.

With some of the required voltage loop compensation components integrated in the regulator, the number of external passive components and PC board area typically necessary in a voltage mode buck converter application are reduced. An LM2854 based regulator design with type III loop compensation can be implemented with as few as eight external components. Only two small size external compensation components are required, similar to that commonly involved with current mode control compensation. Unlike a compensation solution where all the compensation components are integrated, the LM2854 has the flexibility to deal with ceramic and/or electrolytic based load capacitance spanning a wide range of capacitor values.

Lossless cycle-by-cycle peak current limit is used to protect the load from an overcurrent or short-circuit fault, and an enable comparator permits system sequencing or increase of the input UVLO above the nominal 2.7V level. The device is available in a power enhanced HTSSOP-16 package featuring an exposed die attach pad that improves the thermal performance of the regulator.

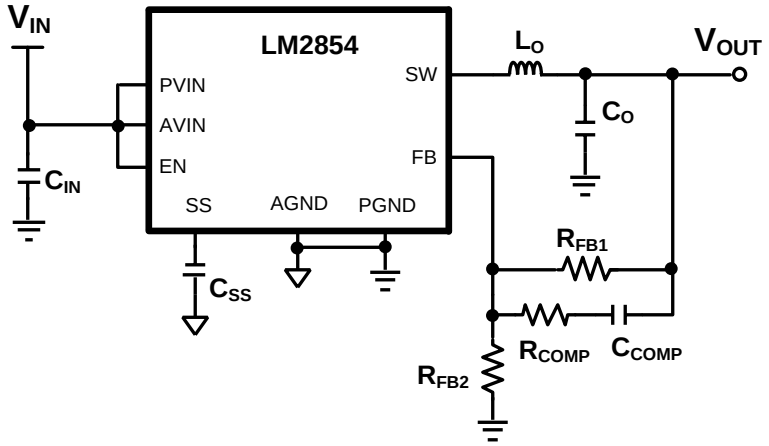

Figure 1. Typical System Application using LM2854 Synchronous Buck Regulator

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2 LM2854 Pin-Out

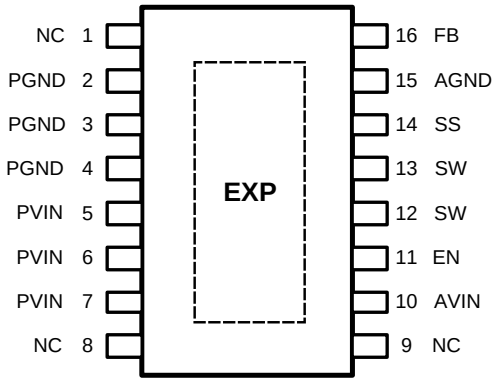

Figure 2. LM2854 Pin-Out

3 LM2854 Pin Descriptions

Table 1. LM2854 Pin Descriptions

Pin Number	Name	Description
1	NC	Reserved for factory use, this pin should be connected to GND to ensure proper operation.
2,3,4	PGND	Power ground pins for the internal power switches. These pins should be connected together locally at the device and tied to the PC board ground plane.
5,6,7	PVIN	Input voltage to the power switches inside the device. These pins should be connected together at the device. A low ESR input capacitance should be located as close as possible to these pins.
8,9	NC	Reserved for factory use, these pins should be connected to GND to ensure proper operation.
10	AVIN	Analog input voltage supply that generates the internal bias. The UVLO circuit derives its input from this pin also. Thus, if the voltage on AVIN falls below the UVLO threshold, both internal FETs are turned off. It is recommended to connect PVIN to AVIN through a low pass RC filter to minimize the influence of input rail ripple and noise on the analog control circuitry. The series resistor should be 1Ω and the bypass capacitor should be a X7R ceramic type 0.1 µF to 1.0 µF.
11	EN	Active high enable input for the device. Typically, turn-on threshold is 1.23V with 0.15V hysteresis. An external resistor divider from PVIN can be used to effectively increase the UVLO turn-on threshold. If not used, the EN pin should be connected to PVIN.
12,13	SW	Switch node pins. This is the PWM output of the internal MOSFET power switches. These pins should be tied together locally and connected to the filter inductor.
14	SS	Soft-start control pin. An internal 2 µA current source charges an external capacitor connected between this pin and AGND to set the output voltage ramp rate during startup. This pin can also be used to configure the tracking feature.
15	AGND	Quiet analog ground for the internal bias circuitry.
16	FB	Feedback pin is connected to the inverting input of the voltage loop error amplifier. A 0.8V bandgap reference is connected to the non-inverting input of the error amplifier.
EXP	Exposed Pad	Exposed metal pad on the underside of the package with a weak electrical connection to PGND. It is recommended to connect this pad to the PC board ground plane in order to improve thermal dissipation.

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4 LM2854 Evaluation Board Schematic

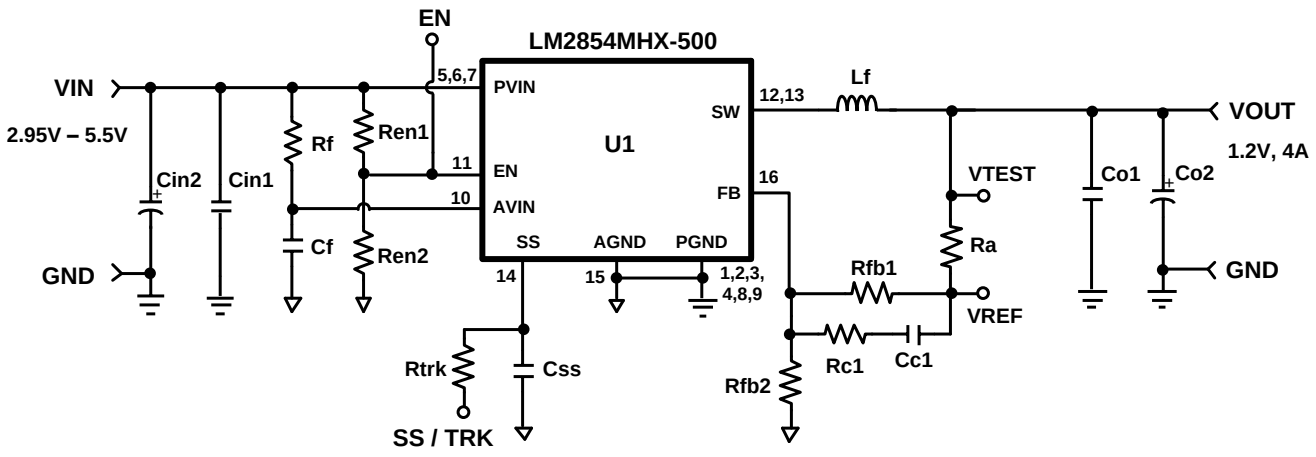

Figure 3. LM2854 Evaluation Board Schematic Diagram

Table 2. LM2854 500 kHz Bill of Materials, V_{IN} = 2.95V to 5.5V, V_{OUT} = 1.2V, $I_{OUT(MAX)}$ = 4A

Ref. Des.	Function	Description	Case Size	Manufacturer	Manufacturer P/N
U1	Regulator	Synchronous Buck Regulator	HTSSOP-16	Texas Instruments	LM2854
Cin1	Input Filter	47 µF, X5R, 10V	1210	TDK	C3225X5R1A476M
Cin2	Input Filter	150 µF, 6.3V	C2 Case	Panasonic	6TPE150MIC2
Co1	Output Filter	100 µF, X5R, 6.3V	1210	TDK	C3225X5R0J107M
Co2	Output Filter	Not Assembled	C2 Case	-	-
Lf	Output Filter	1.5 µH, 14 mΩ	6.9 x 6.5 x 3.0 mm	Vishay	IHLP2525CZER1R5M01
Rfb1	Upper FB Resistor	249 kΩ	0603	Vishay Dale	CRCW06032493F-e3
Rfb2	Lower FB Resistor	499 kΩ	0603	Vishay Dale	CRCW06034993F-e3
Rc1	Compensation Resistor	1.0 kΩ	0603	Vishay Dale	CRCW06031001F-e3
Rf	AVIN Filter Resistor	1.0Ω	0603	Vishay Dale	CRCW06031R0F-e3
Ren1	Enable Resistor	100 kΩ	0603	Vishay Dale	CRCW06031003F-e3
Ren2	Enable Resistor	Not Assembled	0603	-	-
Rtrk	Track Resistor	10 kΩ	0603	Vishay Dale	CRCW06031002F-e3
Ra	Injection Resistor	50Ω	0603	Vishay Dale	CRCW06035000F-e3
Cc1	Compensation Capacitor	47 pF, ±5%, C0G, 50V	0603	TDK	C1608C0G1H470J
Css	Soft-start Capacitor	10 nF, ±10%, X7R, 50V	0603	TDK	C1608X7R1H103K
Cf	AVIN Filter Capacitor	1.0 µF, ±10%, X7R, 16V	0603	TDK	C1608X7R1C105K
TP1,TP2,TP3	Measurement	Scope Probe Connector		Tektronix	131-5031-00

5 LM2854 Evaluation Board Details

This application solution relates to the bill of materials shown in Table 2 and references the schematic diagram in Figure 3 above. The board contains the LM2854MHX-500 buck regulator IC with nominal switching frequency, f_{SW}, of 500 kHz.

6 Quick Step Procedure

1. Set the power supply current limit to 3A. Turn off the power supply. Connect the power supply to the VIN and GND terminals.

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2. Connect the load with a 4A capability to the VOUT and GND terminals
3. The EN terminal can be left open for normal operation as there is an on-board pull-up resistor.
4. Set V_{IN} to 3.0V with no load applied. V_{OUT} should be in regulation with a nominal 1.2V output.
5. Slowly increase the load while monitoring the output voltage. V_{OUT} should remain in regulation with a nominal 1.2V output as the load is increased up to 4A.
6. Slowly sweep the input voltage from 2.95V to 5.5V. V_{OUT} should remain in regulation with a nominal 1.2V output.
7. Temporarily short the EN terminal to GND to check the shutdown function.
8. Increase the load beyond the normal range to check current limit. The output current should limit at approximately 5.6A. Short the VOUT and GND terminals to verify short circuit protection.

7 Component Selection

7.1 Filter Inductor

The selection of the output filter components, Lf and Co1, are intrinsically linked as both of these parameters affect the stability of the system and various characteristics of the output voltage.

First, a 1.5 µH inductor is chosen to allow stable operation (per datasheet recommendations) over the entire input voltage range from 2.95V to 5.5V. The inductance also directly affects the amplitude of the inductor current ripple which flows in the output capacitor. The filter inductance is given by

$$Lf = \frac{V_{OUT}(1-D)}{\Delta i_L f_{SW}} = \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\Delta i_L f_{SW}} \tag{1}$$

where the variable D refers to the duty cycle and can be approximated by

$$D = \frac{V_{OUT}}{V_{IN}} \tag{2}$$

From this, it follows that the inductor ripple current, Δi_L, reaches a maximum when duty cycle is minimum or input voltage is maximum, i.e. V_{IN} = 5.5V. Under these conditions, the inductor peak to peak ripple current is given by

$$\Delta i_L = \frac{1.2V\left(1 - \frac{1.2V}{5.5V}\right)}{1.5\ \mu H \times 500\ kHz} = 1.25A \tag{3}$$

or approximately 31% of full load current. It follows that the peak inductor current at full load is

$$I_{Lpk} = I_{OUT} + \frac{\Delta i_L}{2} = 4A + \frac{1.25A}{2} = 4.63A \tag{4}$$

and this level is adequately below the peak inductor current associated with current limit. This implies that an inductor must be selected with a saturation current higher than 4.63A to ensure that the inductor will never saturate during normal operating conditions.

Another concern related to the inductance value is that it governs the maximum inductor current slew rate during a load on or off transient respectively as follows

$$\left.\frac{di_L}{dt}\right|_{UP} = \frac{(V_{IN} - V_{OUT})}{Lf}$$
$$\left.\frac{di_L}{dt}\right|_{DOWN} = \frac{V_{OUT}}{Lf} \tag{5}$$

Thus, a smaller inductance value allows the control loop to slew the inductor current more rapidly.

This evaluation board uses the Vishay IHLP2525 series 1.5 µH inductor to provide the necessary current handling capability with low DC resistance in a relatively small footprint and profile .

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7.2 Output Capacitor

The output capacitance and its equivalent series resistance (ESR) affect both the ripple voltage at the output and the overall stability of the loop. The output capacitor provides a low impedance path for the inductor ripple current and presents a source of charge for transient loading conditions.

In this example, one 100 µF 1210 multi-layer ceramic capacitor (MLCC) was selected. Ceramic capacitors provide very low ESR but can exhibit a significant reduction in capacitance with applied DC bias. Using manufacturer's data, the ESR at 500 kHz is 3 mΩ and there is approximately 40% reduction in capacitance at 1.2V. This is verified by measuring the output ripple voltage and frequency response of the circuit. The fundamental component of the output ripple voltage amplitude is calculated as

$$\Delta V_{OUT} = \Delta i_L \sqrt{R_{ESR}^2 + \left(\frac{1}{8 f_{SW} C_O 1}\right)^2} \tag{6}$$

and with typical values from this example

$$\Delta V_{OUT} = 1.25A \sqrt{(3\ m\Omega)^2 + \left(\frac{1}{8\ 500\ kHz\ 60\ \mu F}\right)^2} = 6.4\ mV \tag{7}$$

Because the load could transition quickly from no load to full load, it is sometimes common to add output bulk capacitance in the form of aluminum electrolytic (Al-E), tantalum (Ta), solid aluminum, organic polymer, and niobium (Nb) capacitors. This is largely unnecessary with the LM2854 as the loop crossover frequency can be made sufficiently large to accommodate high di/dt load transients.

7.3 Input Filter

The necessary RMS current rating of the input capacitor can be estimated by the following equation

$$I_{Cin(RMS)} = I_{OUT}\sqrt{D(1-D)} \tag{8}$$

From this equation, it follows that the maximum RMS current will occur at full 4A load current with the system operating at 50% duty cycle.

However, with the specified output voltage, the worst case occurs at minimum input voltage of 2.95V. Hence, the relevant duty cycle is 0.41 and the maximum RMS current is given by

$$I_{Cin(RMS)} = 4A\sqrt{0.41\ (1 - 0.41)} = 1.97A \tag{9}$$

Ceramic capacitors feature a very large RMS current rating in a small footprint making them ideal for this application. Choosing a 47 µF 10V ceramic capacitor to provide the necessary input capacitance and assuming 50% capacitance voltage coefficient, the input AC ripple amplitude, neglecting ESR, is

$$\Delta V_{IN} = \frac{I_{OUT} D(1-D)}{f_{SW} Cin1} = \frac{4A\ 0.41\ (1 - 0.41)}{500\ kHz\ 24\ \mu F} = 80\ mV \tag{10}$$

When operating near the minimum input voltage, an electrolytic input capacitor is helpful to damp the input for a typical bench test setup. Essentially, a resonant circuit is formed by the line impedance and input capacitance. To this end, a second input capacitor, Cin2, is provided on the evaluation board to accommodate such electrolytic capacitance. The 6TPE150MIC2 by Sanyo has 150 µF capacitance and an ESR of 18 mΩ. The associated ESR is stable relative to temperature, and capacitance change is relatively immune to bias voltage. The ripple current will split between the ceramic and electrolytic capacitors based on the relative impedance at the switching frequency.

For improved performance, an 0603 1 µF ceramic AVIN filter capacitor is placed adjacent to the AVIN pin and referenced to AGND. Together with a 1Ω series resistor from PVIN (optional), this small capacitor helps to filter high frequency noise spikes on the supply rail and prevent these pulses from disturbing the analog control circuitry of the chip.

7.4 Soft-Start Capacitor

A 10 nF soft-start capacitor has been chosen to provide a soft-start time of roughly 4 ms. This will allow the LM2854 to start up gracefully without triggering over-current protection irrespective of operating conditions.

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7.5 Tracking Resistors

If simultaneous (equal voltage ramp rates) or ratiometric (equal soft-start times) tracking to an external supply voltage, V_{TRACK}, is required, the user can remove the soft-start capacitor and replace with the appropriate value lower tracking resistor. The upper resistor, Rtrk, is 10 kΩ. Thus, the lower tracking resistor value, designated Rtrk1, is governed by

$$Rtrk1 = \begin{cases} \dfrac{10\ k\Omega}{(V_{TRACK} - 1.0V)}, \text{ Simultaneous Tracking} \\ \dfrac{0.8V}{(V_{OUT} - 0.8V)} 10\ k\Omega, \text{ Ratiometric Tracking} \end{cases} \tag{11}$$

7.6 Enable Resistors

The LM2854 has an enable pin with an on-board 100 kΩ pull-up resistor, designated Ren1. Thus, the associated PCB terminal, labeled EN, can be left open circuit if desired. Alternatively, the enable function can be configured to increase the input UVLO level by setting up a resistor divider from VIN using resistors Ren1 and Ren2. The board is supplied with Ren2 not assembled.

7.7 Feedback and Compensation Components

The voltage loop crossover frequency, f_{loop}, is usually selected between one tenth and one fifth of the switching frequency

$$0.1\ f_{SW} \le f_{loop} \le 0.2\ f_{SW} \tag{12}$$

The complex double pole related to the LC output filter and zero due to the output capacitor ESR are as follows

$$f_{LC} \cong \frac{1}{2\pi\sqrt{LfCo1}} = \frac{1}{2\pi\sqrt{1.5\ \mu H\ 60\ \mu F}} = 16.8\ kHz$$

$$f_{ESR} \cong \frac{1}{2\pi\ R_{ESR}Co1} = \frac{1}{2\pi\ 3\ m\Omega\ 60\ \mu F} = 885\ kHz \tag{13}$$

A simple solution for the required external compensation capacitor, C_{COMP}, with type III voltage mode control can be expressed as follows where the constant is nominally 0.038 for the 500 kHz option.

$$Cc1(pF) = \alpha\ \frac{Lf(\mu H)Co1(\mu F)}{V_{IN}\ (V)}\ f_{loop}\ (kHz)$$

$$Cc1 = 0.038\ \frac{1.5\ 60}{5.5}\ 75 = 47\ pF \tag{14}$$

The upper feedback resistor, Rfb1, is selected to provide adequate mid-band gain and to locate a zero at or below the LC pole frequency. The series resistor, Rc1, is selected to locate a pole at the ESR zero frequency. Thus

$$Rfb1 = \frac{1}{2\pi Cc1 f_{LC}} = \frac{1}{2\pi\ 47\ pF\ 16.8\ kHz} = 200\ k\Omega$$

$$Rc1 = \frac{1}{2\pi Cc1 f_{ESR}} = \frac{1}{2\pi\ 47\ pF\ 885\ kHz} = 3.8\ k\Omega \tag{15}$$

Rfb1 and Rc1 are chosen as 249 kΩ and 1 kΩ in the evaluation board. With Rfb1 defined based on the voltage loop requirements, Rfb2, the lower feedback resistor, is then selected for the desired output voltage by

$$Rfb2 = \frac{Rfb1}{\left(\frac{V_{OUT}}{0.8V} - 1\right)} = \frac{249\ k\Omega}{\left(\frac{1.2V}{0.8V} - 1\right)} = 499\ k\Omega \tag{16}$$

Note that Rfb2 has no impact on the control loop from an AC standpoint since the FB pin is the input to an op-amp type error amplifier and effectively at AC ground. Hence, the control loop can be designed irrespective of output voltage level. The only caveat here is the necessary derating of the output capacitance with applied voltage.

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The compensation was optimized to work over the full input voltage range. Many applications have a fixed input voltage rail. It is possible to modify the compensation to obtain a faster transient response for a given input voltage operating point .

8 Performance Characteristics

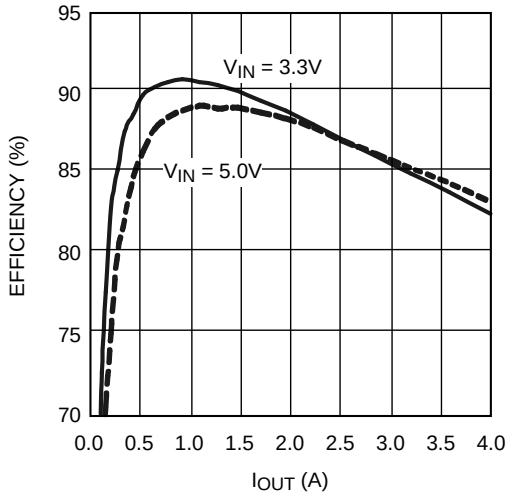

Figure 4. LM2854 Evaluation Board Efficiency
V_{OUT} = 1.2V

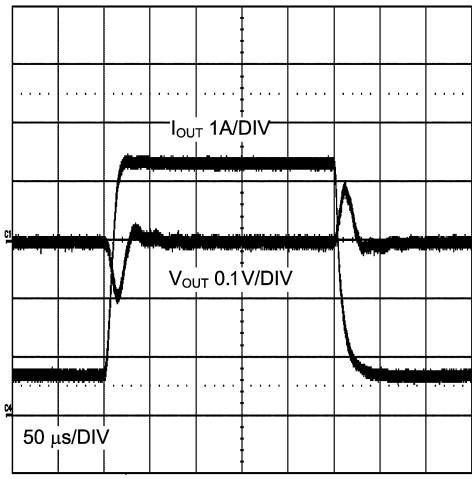

Figure 5. LM2854 Transient Response
I_{OUT} = 0.4A - 4.0A - 0.4A

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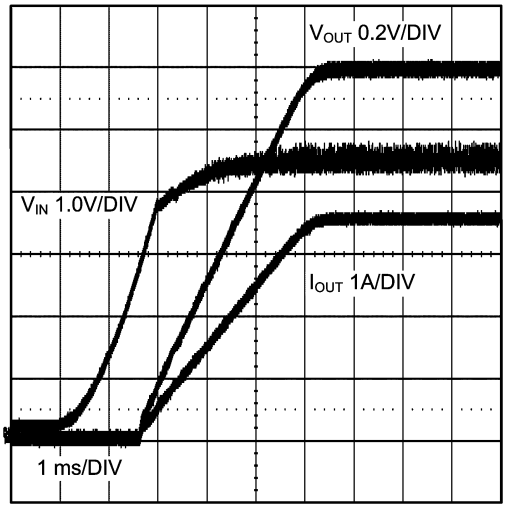

Figure 6. LM2854 Startup Characteristic

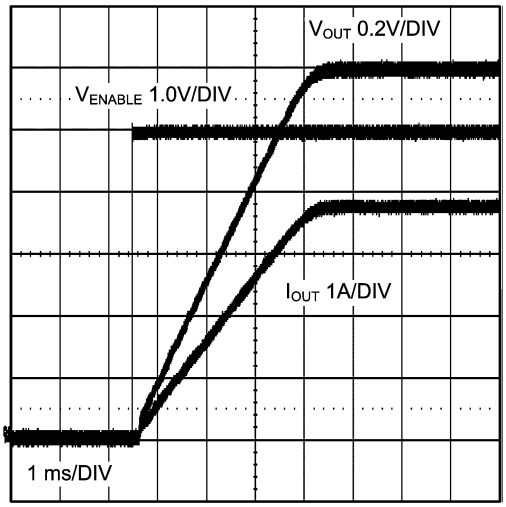

Figure 7. LM2854 Turn On via Enable

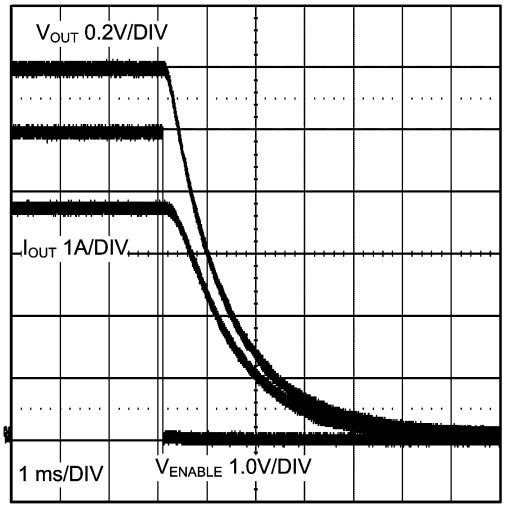

Figure 8. LM2854 Turn Off via Enable

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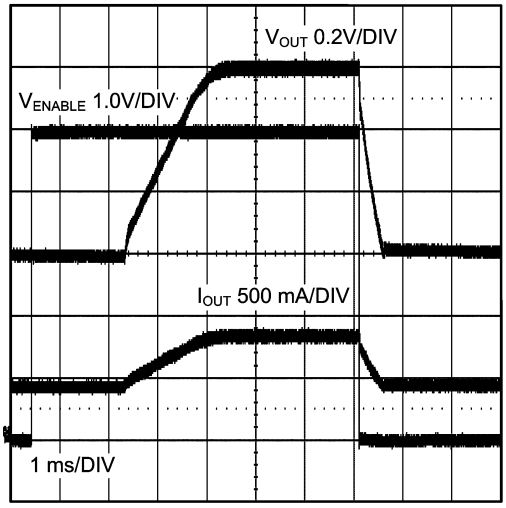

Figure 9. LM2854 Pre-BiasedTurn On and Off via Enable $V_{OUT(PRE-BIAS)}$ = 0.6V

9 LM2854 PC Board Layout

The evaluation board is based on a small 2.0” x 1.2” x 0.062” (51 mm x 31 mm x 1.6 mm) FR4 laminate PCB with two layers of two ounce copper. The top and bottom side layouts can be seen in Figure 5 and Figure 6 below. When looking at the top layer, pin 1 of the LM2854 is on the upper left.

Three Textronix oscilloscope probe connectors are provided to facilitate convenient measurement of V_{IN}, V_{OUT} and V_{SW} (switch node). Furthermore, a 50Ω series resistor, assigned reference designator Ra, is provided that appears in series with the V_{OUT} sense trace. This component and associated connectors are provided to give the user maximum flexibility and enable a convenient point for oscillator signal injection during loop bode plot measurements.

The PCB layout of the LM2854 evaluation board was designed to occupy as little board space as possible, while still following sound layout guidelines and techniques. The input capacitor, Cin1, is placed as close as possible to the PVIN and PGND pins to minimize stray resistance and inductance between Cin1 and the LM2854. Likewise, the AVIN bypass capacitor is placed as close as possible to the AVIN and AGND pins. PGND and AGND are connected to each other and the ground plane at a single point, the exposed pad of the LM2854.

Also, in order to help conduct heat to the ground plane and away from the LM2854, a 3 x 3 via array is used to electrically and thermally connect the exposed pad to the ground plane (instead of a single via). Additional ground plane vias are located close to the three PGND pins and in the localized ground plane emanating away from the exposed pad.

Finally, the FB pin trace is intentionally kept as short as possible and routed away from the SW node to minimize any EMI pickup.

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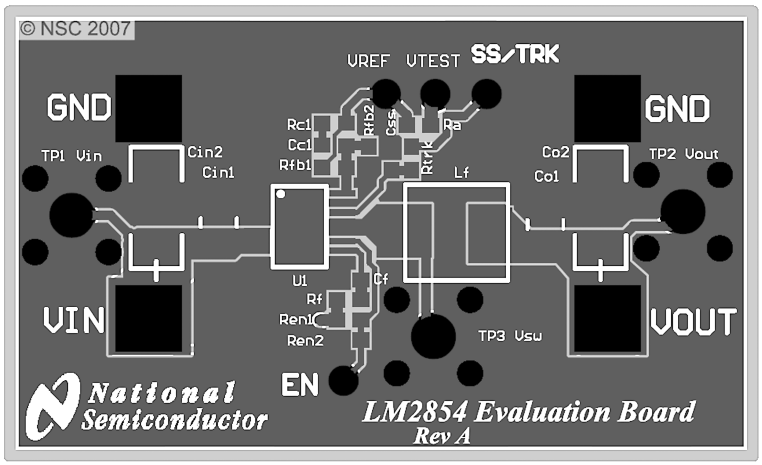

Figure 10. LM2854 Top Side PCB Layout

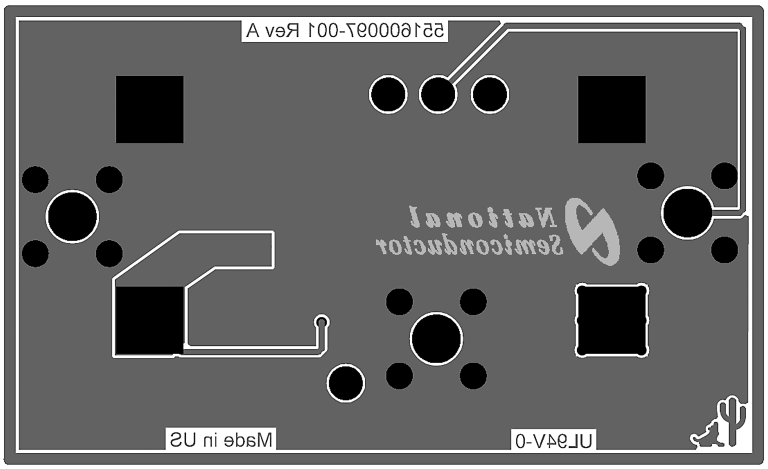

Figure 11. LM2854 Bottom Side PCB Layout, Viewed from Top

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Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
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